Assassyn: A Unified Abstraction for Architectural Simulation and Implementation

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Abstract

The continuous growth of on-chip transistors driven by technology scaling urges architecture developers to design and implement novel architectures to effectively utilize the excessive on-chip resources. Due to the challenges of programming in register-transfer level (RTL) languages, performance modeling based on simulation is typically developed alongside hardware implementation, allowing the exploration of high-level design decisions before dealing with the error-prone, low-level RTL details. However, this approach also introduces new challenges in coordinating across multiple teams to align implementation details separate codebases.

In this paper, we address this issue by presenting Assassyn, a *unified*, *high-level*, and *general-purpose* programming framework for architectural simulation and implementation. By taking advantage of the concept of asynchronous event handling, a widely existing behavior in both hardware design and implementation and software engineering, a *general-purpose*, and *high-level* programming abstraction is proposed to mitigate the difficulties of RTL programming. Moreover, the *unified* programming interface naturally enables an accurate and faithful alignment between the simulation-based performance modeling and RTL implementation.

Our evaluation demonstrates that Assassyn's high-level programming interface is sufficiently expressive to implement a wide range of architectures, from architectural components, and application-specific accelerators, to designs as complicated as out-of-order CPUs. All the generated simulators perfectly align with the generated RTL behavior, while achieving 2.2-8.1× simulation speedup, and requiring 70% lines of code. The generated RTL achieves comparable perf/area compared to handcrafted RTL, and 6× perf/area compared to high-level synthesis generated RTL code by introducing by mean 1.26× lines of code overhead.

CCS Concepts

• **Hardware** → **Hardware description languages and compilation**; • **Computer systems organization** → *High-level language architectures*; *Data flow architectures*; *Pipeline computing*.

Keywords

Performance Modeling and Simulation, Open-source Hardware, High-level Hardware Description Language

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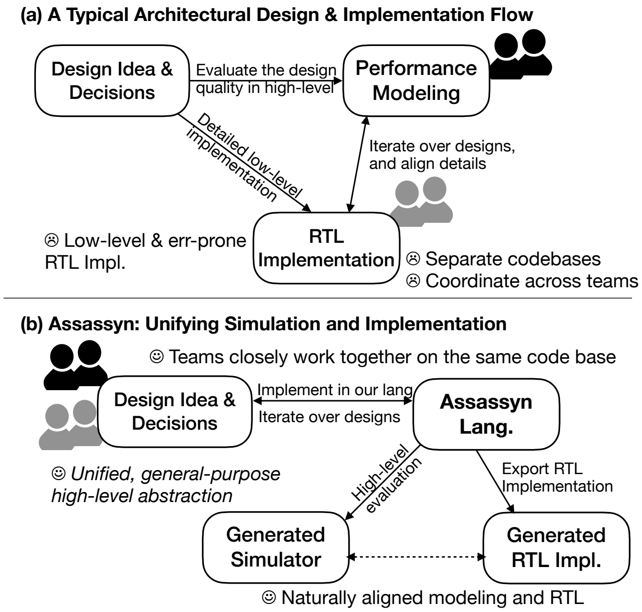


Figure 1: A typical flow of architectural design and implementation compared to our goal, designing and implementing in a *unified, high-level, and general-purpose* interface.

1 Introduction

Technology scaling continues to provide abundant on-chip transistors, urging developers to create innovative architectures to effectively utilize these resources. These architectural innovations have attracted significant attention from both industry and academia for their potential to deliver remarkable performance gains and energy efficiency. However, realizing these innovations is no small feat; as shown in Figure 1(a), transforming an architectural design into a hardware implementation demands a lengthy and complex process involving collaboration across multiple teams. The excessive low-level details exposed by Register-Transfer Level (RTL) language significantly hinder the design space and decision exploration of an architecture. To address this, simulation-based performance models are often developed alongside hardware implementations, so that high-level design ideas and decisions can be evaluated before confronting the challenges of error-prone RTL language.

However, this two-pronged approach introduces a significant challenge: maintaining and aligning simulation-based modeling and RTL implementation of the target architecture imposes substantial coordination burdens across multiple teams. This difficulty stems from using different codebases and programming languages for performance modeling and RTL implementation, leading to potential inconsistencies and increased development time.

Prior works [5, 7, 10, 11, 13, 16, 19, 21, 23–26, 29, 31, 33–35, 37, 40, 41, 45, 49, 52–54, 60, 62–64, 66, 69, 70, 75, 76, 79, 81] [1] follow this design and implementation paradigm, reporting performance numbers from simulation-based modeling, and the power/area evaluations from separate synthesized RTL implementations. However, the alignment between the simulation and hardware implementation is often overlooked, highlighting a persistent challenge of this two-pronged approach.

Our Goal (cf. Figure 1(b)): Recognizing these limitations in current practices, we propose that an ideal architectural design and implementation workflow shall have a *unified, general-purpose, and high-level* language to describe the architecture design to generate both cycle-accurate simulation and RTL implementation. This approach enables multiple teams to collaborate closely, iterating on high-level design decisions and implementation details together, while seamlessly maintaining alignment between performance modeling and RTL implementation. The generated RTL implementation should have minimized overhead caused by high-level abstraction. Prior works [27, 65, 68, 72] automate architecture design and implementation by adopting *high-level* programming interfaces that *unify* the software development and hardware generation; however, they all failed to be *general-purpose* — their target application domain or underlying hardware is limited within a designated scope.

Our Approach: In light of these limitations, we propose Assassyn[2], a fundamentally different approach that *unifies* the *general-purpose* hardware design and implementation in a *high-level* programming abstraction. Our approach is enabled by generalizing the hardware's behaviors: Pipelined designs are widely adopted to improve the performance and frequency in modern architectures, and our insight is that both simulating and implementing such pipelined architectures can be abstracted as *asynchronous event handling*. By leveraging several widely adopted concepts in functional programming (high-order functions and bind) and software engineering (async event handling), a *high-level and general* language for pipelined hardware description is developed to better manage the error-prone and tedious efforts in RTL programming, and explore the high-level design parameters decoupled from the architectural designs. The key contributions of Assassyn are:

- Recognizing a generalized paradigm for pipelined architectures' design and implementation.
- Based on this generalized paradigm, a *unified, high-level, and general-purpose* programming language is proposed for hardware simulation and implementation. To the best of our knowledge, this is the **first** RTL generator that is both *high-level, and general-purpose.*
- By integrating a fully open-source workflow, from frontend language to synthesis tool, and technique library, an end-to-end flow is presented to maximize the reproducibility of architectural research.

Our evaluation shows that Assassyn's programming abstraction is: 1. highly productive to easily target architecture designs and implementations while requiring only 70% of lines of code; 2. sufficiently expressive to target diverse prior designs, from design components to end-to-end accelerators and CPUs; 3. efficient to generate RTL implementation with comparable quality compared to handcrafted designs.

The rest of the paper is organized as follows: the backgrounds on the existing approach on hardware design and implementation will be overviewed in Section 2 to motivate our approach; the technical

[1] All these papers are from a single conference proceedings, ISCA 2024.

[2] Assassyn is the acronym for asynchronous semantics for architectural simulation and synthesis.

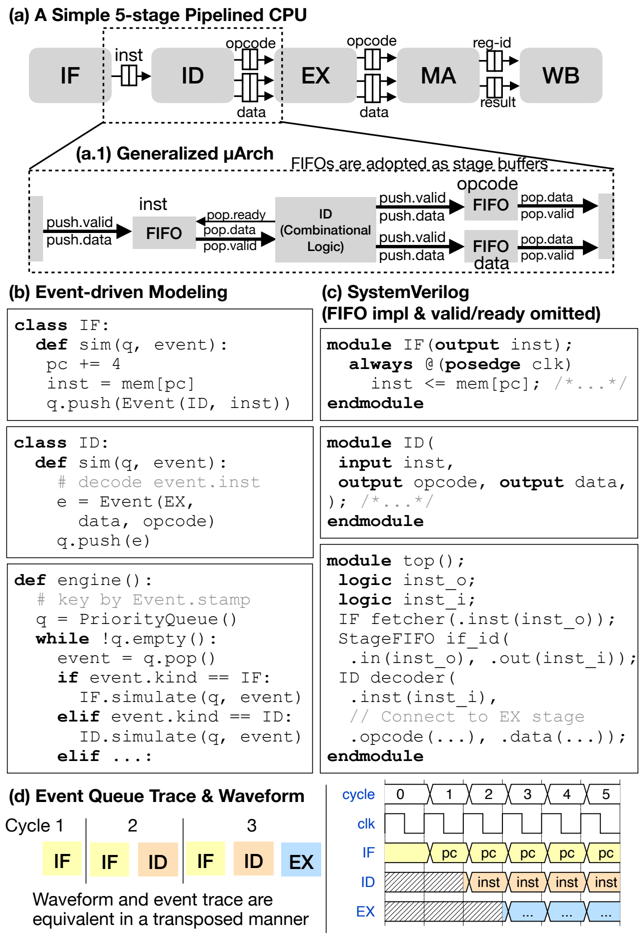


Figure 2: A 5-stage pipeline evaluated in both an event-driven simulator, and an RTL simulator.

details of Assassyn will be explained in in Section 3, 4, and 5, including the programming abstraction, compiler transformations, and the runtime and μ-architectural support. Finally, the experiment setup and the evaluation will be presented in Section 6 and 7 so that we can discuss and conclude this work in Section 8.

2 Background & Motivation

In this section, we first overview the existing technologies for hardware modeling and implementation, highlighting their challenges and opportunities, to motivate our proposed *unified, high-level, and general-purpose* programming interface for both simulation-based modeling, and pipeline description.

2.1 Pipeline Design & Implementation

Pipelining is widely adopted in modern architectures to improve the performance by separating interdependent logic into multiple stages, so more transistors remain active simultaneously. While promising, this architectural paradigm imposes additional implementation challenges in managing the communications and timing among pipeline stages. To mitigate these challenges, before engaging with these low-level and error-prone details exposed in the RTL

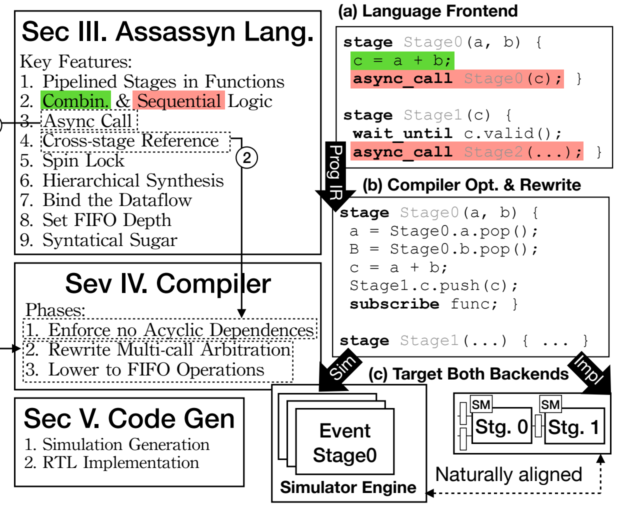


Figure 3: An overview to Assassyn.

language, simulation-based performance models are often built alongside to explore the high-level design decisions.

Simulation-based Hardware Modeling: Many prior works' performances were modeled by either implementing in-house [11, 19, 23, 29, 62] or extending existing open-source [9, 14, 30, 36, 48, 61] simulators. These *simulation-based* models provide detailed performance insight into the architectural pipeline by tracking the state and behaviors of each pipeline stage in each cycle.

As illustrated in Figure 2(b), event-driven simulation is a typical approach of simulating a 5-stage CPU pipeline by maintaining an event queue. Each stage's functionality is simulated by popping and processing the corresponding event. Notably, each stage triggers the next stages by pushing an event instance associated with its inputs to the queue, which is similar to *asynchronously* invoking a function. For example, the `IF` stage enqueues an event for the `ID` stage with fetched instruction associated, while `ID`'s simulation will not be occur until the next cycle, which is akin to invoking `ID.sim` *asynchronously*.

The event engine terminates once the queue is empty, or it reaches a predefined cycle threshold. This simulation-based approach allows developers to rapidly explore design ideas and decisions at a high level, but unrealistic assumptions may significantly compromise the accuracy of simulation results [51]. In addition, the fundamental differences between the programming models cause a nontrivial effort to bridge the simulated designs to actual RTL implementations.

Hardware Implementation: To mitigate the difficulties in programming low-level RTL language, prior works automate architecture design and implementation by trading off the generality. For instance, with a designated architectural paradigm, highly specialized designs can be generated for the given sets of the target applications, by tuning the parameters and adjusting the topology of the template architecture [39, 56, 72]. Some other works [27, 65, 68] focus on particular application domains or constructs, such as perfect loop nests, allowing these frameworks to achieve performance comparable to or even surpassing hand-crafted designs. However, when an application or architecture design falls outside the framework scope, developers must either extend the framework to accommodate new designs or revert to manual implementations.

A RTL language, such as SystemVerilog, offers full control over the underlying hardware implementation, from the circuit structure to the cycle timing. While this fine-grain control is necessary for many optimal designs, exposing excessive low-level details also make the programming process complex and error-prone. Commercial and open-source RTL projects, like Bluespec Verilog [1], and Chisel [6], attempted to alleviate these difficulties by offering syntactic sugar and encapsulated APIs, but still, these tools adhere closely to the RTL's programming and execution model, leaving the fundamental challenges on dealing with timing, concurrency, and cycle-carried state machines unresolved.

Challenges and Opportunities: In contrast to event-driven simulation, which *pushes* data forward through pipeline stages, RTL programming follows an event-listen paradigm where stages *pull* in data to process their state machines. Figure 2(c) shows the `IF` stage listens to `clk` signal to fetch instructions, and the `ID` stage listens to fetched `inst` from `IF`. This *pull/push* mismatch creates a significant gap between architecture design and implementation. However, Figure 2(d) suggests that there exists a fundamental correspondence between simulation traces and waveforms when viewed in a transposed manner. This correspondence presents an opportunity to create a unified abstraction to bridge the simulation and RTL implementation.

2.2 Event-driven Programming

Based on the correspondence between the event trace and the RTL waveform, accompanied with the asynchronous event-driven nature in hardware simulation, we motivate an asynchronous event-driven programming abstraction to bridge the architectural simulation and implementation. Before introducing this programming abstraction in the next section, we first formalize a generalized architecture pipeline model and relate this model to event-driven programming.

Asynchronous Event-handling & Pipeline Stages: An asynchronous event is executed when its corresponding entry in a bookkeeping FIFO is scheduled. Pipeline stage activation can be abstracted as asynchronous event handling in a similar mechanism: When a pipeline stage is called, its bookkeeping state machine is *subscribed*. This *subscription* remains until the stage is activated, at which point it is cleared. Moreover, the boundary between synchronous and asynchronous execution naturally defines the scope of timing.

Cycle-bound Timing: In Assassyn, each pipeline stage naturally defines a cycle-bound scope. Within each pipeline stage, everything is done in the "current cycle", and the asynchronously invoked stage will be executed no earlier than the "next cycle". For example, Figure 2(d) shows that each pipeline stage is executed in a cycle-bound manner: each pipeline stage is finished within the current cycle, and the enqueued new events will not be executed until next cycle. Moreover, the transposed event-waveform correspondence revealed in this figure also implies a perfect cycle alignment between simulation-based modeling and RTL simulation.

Dataflow across Stages: In architecture design, data flows from one stage to another, which is analogous to a function call: a stage (callee) takes inputs from upstream (caller) and produces outputs for downstream stages (recursively invoke another callee). However, a key distinction between software programming and hardware design is that data for callee in software are typically all from a single caller. In contrast, a pipeline stage can accept data from multiple upstream stages. This multi-source data flow can be abstracted as function bind (see Listing 1), which is is also known as `functools.partial` in Python. This language feature fixes a subset of the function arguments, and creates a new function with fewer arguments.

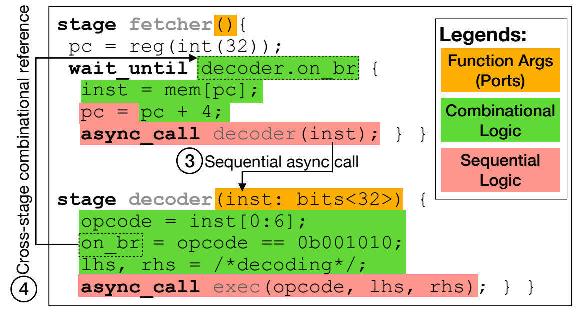


Figure 4: Pipeline stages, IF, and ID, programmed in Assassyn.

```
from functools import partial
def foo(x, y): return x + y
goo = partial(foo, 5) # Fix foo.x = 5
goo(10) # Equivalent to foo(5, 10)
```

Listing 1: A function bind example.

Note, this `bind` approach is **not** a syntactical sugar. This abstraction significantly improves the expressiveness. Refer to Figure 5(b) and explanations in Section 3.7 for more details on how this is used for dataflow abstraction.

Generalized Architectural Pipeline: As it is shown in Figure 2(a.1), an architectural pipeline can be generalized as follows: reading data from the upstream stage buffers, processing them through the intra-stage combinational logic, and then pushing the results to downstream stage buffers. This generalized flow captures the essence of a pipelined architecture. After decades of research and evolution, we believe that the communication protocols and signal-handling mechanisms between pipeline stages have converged toward several mature and optimal design patterns. In our design, we adopt a simple FIFO structure for stage buffers/stage registers, chosen for its balance between generality, efficiency, and moderate on-chip area requirements. For more details on the microarchitectural support and automatic code generation, please refer to Section 5.

All the technical aspects of Assassyn, as well as the synergies among them, are overviewed in Figure 3. In the following three sections, we will in detail explain each of them.

3 Assassyn: Abstraction & Syntax

In this section, we will in detail explain Assassyn's abstraction to describe a pipelined architecture in a *high-level, and general-purpose* programming interface for both cycle-accurate simulation, and RTL generation by sticking to the examples shown in Figure 4 and 5.

3.1 Program pipeline stages in functions

Functions serve as the most fundamental building block of Assassyn to construct each stage of a pipelined architecture. Each function consists of a unique identifier to reference this function itself, an argument list for the stage inputs, and the combinational and sequential logic within its body. Only arithmetic operations, and conditional statements (i.e. if&select) are supported in the function bodies. No loops are supported in function bodies. This restriction ensures that there are no cyclic dependences among the combinational logic within each function to maintain the necessary acyclic nature for proper hardware synthesis. Each function corresponds to dedicated on-chip recourses when synthesized, establishing a direct mapping from our high-level language constructs to physical hardware components.

3.2 Separate combinational & sequential logic

The scope of a function naturally establishes a clear boundary between combinational and sequential logic: all arithmetic computations performed synchronously within this function are considered combinational, which can be completed within one cycle, while any side-effect operations (such as register updates, and memory write) are sequential. These side-effect operations will take effect in the next cycle, which reflects the inherent timing behavior. As shown in ① of Figure 4 activating a downstream stage is sequential, because it involves stage register, state machine writings. The μ-architectural support for the stage registers and state machines will be in detail explained in Section 5.2.

3.3 Invoke stages asynchronously

As discussed in Section 2.2, asynchronous function calls naturally capture the hardware behavior of stage activation — each stage operates on the output of the previous stage in the subsequent clock cycle. As it is shown in Figure 4, the `fetcher` activates the `decoder` stage by calling `decoder` asynchronously, and `decoder` in turn calls `executor` with the decoded results. This chain of asynchronous calls models the flow of data through the pipeline stages, with each stage processing its input in one clock cycle and passing the results to the next stage to be processed in the following cycle. As overviewed in ① of Figure 3, Section 4.3 will elaborate on how the compiler lowers asynchronous function calls for code generation.

3.4 Reference cross-stage logic

In contrast to conventional RTL syntax, where exposing a value to an external module requires verbose module instantiation and explicit pin connections, our language supports a straightforward cross-stage value reference by directly accessing a variable within another function body. As shown in○ of Figure 4, a combinational logic `decoder.on_br` is directly accessed to immediately determine either to fetch a new instruction or stall. The compiler will automatically determine the type of logic of the cross-stage referenced value. See Section 3.7 for an example of cross-stage sequential reference. As overviewed in ② of Figure 3, Section 4.1 provides more details on how the compiler enforces acyclic dependencies among combinational logic.

3.5 Wait until the spin is unlocked

To provide fine-grained control over the execution of invoked functions, we introduce the `wait_until` statement. This statement primitive allows a callee function to postpone its execution until a specified condition is satisfied. When a caller asynchronously invokes a callee, the callee maintains a bookkeeping mechanism to track incoming asynchronous calls. If there is at least one pending call, the callee function continuously checks its wait-until condition to determine whether it should execute, which works like a *spin lock*. If the condition evaluates to true, the function executes and clears the bookkeeping; if not, it defers execution, retaining the count of pending calls until the condition becomes true. All the unused data will be buffered in stage registers, and multiple invocations will be managed by compiler-generated arbiter. Refer to Section 5.2 and 4 for more details. For example, in Figure 4, the fetcher stage must wait to fetch new instructions when the decoder detects a branch instruction, preventing the pipeline from fetching incorrect instructions and ensuring correct control flow.

Takeaway: These basic primitives discussed above already enable productive pipeline construction. Next, we will introduce several advanced language features to further improve the expressiveness, code reusability, and design modularity.

3.6 High-order function for duplication

In RTL programming, it is normal to duplicate code for similar modules, typically achieved through parameterized hierarchical synthesis. Since we already use functions to program pipeline stages, it is intuitive to employ *higher-order functions* to parameterize functions. *Higher-order functions* are functions that return parameterized functions by giving different arguments. Consider the Python example below. `foo` will return a two-argument function, which sums up these two arguments and adds another constant `delta`, and this constant `delta` can be parameterized.

```
def foo(delta):
  return lambda x, y: x + y + delta
goo = foo(5); goo(1, 2) # 1 + 2 + 5
```

Listing 2: An higher-order function example.

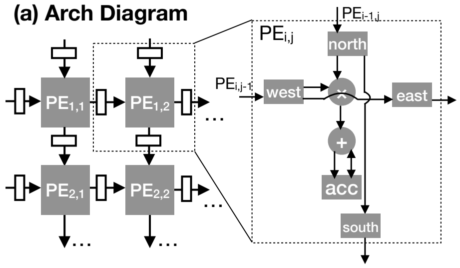
Similarly, in Assassyn, an additional argument list is introduced to instantiate functions with the given argument list which defines the signature of the instantiated function. As shown in Figure 5(b), each systolic processing element is constructed from top-left (1,1) to lower-right (n,n) by supplying its neighbor PEs (south, and east) as parameters. To fully explain this example, the semantics of the `bind` keyword will be discussed in the next section.

3.7 Bind the dataflow

As mentioned, unlike software function calls where all arguments for a callee are provided by a single caller, a pipeline stage often receives data flowed from multiple upstream stages. For example, in the systolic array shown in Figure 5(a), each (PE) receives inputs recursively from its northern and western neighbors–no single PE can asynchronously invoke another with all the necessary data. To address this challenge, we introduce function `bind`, similar to the `functools.partial` in discussed above in Listing 1, which fixes certain arguments of a function in advance, effectively managing partial dataflow from multiple sources.

Figure 5(b) shows how `bind` can be applied to asynchronous function calls, when constructing the entire systolic array. For $\mathrm{PE}_{i,j}$, its southern neighbor's, $\mathrm{PE}_{i+1,j}$, northern input is bound (Figure 5(b), line 8). As illustrated in Figure 5(c), recursively, the eastern $\mathrm{PE}_{i,j+1}$'s northern input is already bound on iteration $i-1$, j. Using the cross-stage access feature discussed in Section 3.4, we can access this bound handle and asynchronously call it (Figure 5(b) line 7) to activate the downstream stage. This approach not only streamlines

(a) Arch Diagram



(b) Higher-order Stage Function

Legend: Higher-order Arguments

```
[#static_timing]
stage PE
   (east:PE,south:bind)
   (west:int<32>,north:int<32>) {
 acc = reg(int(32));
 delta = west * north;
 acc = acc + delta;
 async_call east(west=west);
 bound = bind south(north=north); }
```

(c) Top Function Instantiation

```
1 # Assuming 1-based array, and we
2 # have sentinels for row5 & col5
3 sa = [PE() array of 5x5];
4 # Recursively connect each PE
5 for i in 1..4: for j in 1..4:
6  sa[i][j] = PE.build(sa[i+1][j],
7                      sa[i][j+1].bound)
8  sa[I][j].fifo_depth(west=1,north=1)
```

Figure 5: A systolic array example for hierarchical synthesis, and function bind.

the construction of the systolic array but also simplifies the management of complex *dataflows* among PEs. For more details on the `.build` method, refer to the next section.

3.8 Drive the testbench

To support a testbench function, we reserve the `driver` identifier. When present, the pipeline stage corresponding to this function will be unconditionally activated every cycle, so that this stage can serve as the testbench to generate the signal that *drive*s the execution of the entire pipelined architecture.

3.9 Set the FIFO depth

As discussed in Section 2, to keep the generality of the language, we use FIFOs as our stage registers. Currently, we leave the responsibility of tuning the sizes of the stage FIFOs to the developers through the `fifo_depth` API, as demonstrated in the line 8 of Figure 5(c).

3.10 Syntactical Sugar

Decoupled declaration and implementation: To further explain the systolic array example, we decouple the declaration and implementation of each PE. In complex designs, cyclic dependences among stages may prevent developers from finding a linear order to instantiate each stage. By decoupling declaration and implementation, we can first declare the functions without immediately defining their body logic. Since the function signatures are already determined, only the signatures are needed when constructing the top function. We can instantiate all the functions without concerning for the order of their implementation. Line 3 of Figure 5(c) declares an array of `PE` objects. The internal behavior of each PE is determined by calling the method `.build`, supplying parameters for the higher-order function argument list.

Takeaway: Decoupled declaration and implementation simplifies the management of complex interdependences among the stages.

```
struct Entry {
 valid: bits(1), payload: bits(32) }
# a, b are identical
a, b = reg(Entry), reg(bits(32))
# equivalent to a[0:0] ? a[1:33] : 0
c = a.valid ? a.payload : 0;
# use b like a
d = entry.create_view(a)
e = b.valid ? b.payload : 0;
```

Figure 6: An example for the "struct" syntactical sugar.

Struct slicing: In hardware design, it is normal to pack multiple fields into a bit vector. To simplify access to these packed fields, we introduce a syntactic sugar that allows developers to reinterpret a bit vector as a struct and access its fields through implicit slicing. Figure 6 shows the usage of this syntactical sugar, this struct type can be used to directly declare a data array or create a "view" of an existing bit vector, enabling convenient field-wise access without manual bit manipulation.

4 Compiler

The programmed hardware design undergoes an elaboration process to generate an intermediate representation (IR), a data structure that captures all the aspects of the design. This IR is fed to our compiler to first **enforce** the hardware synthesis constraints. If all the constraints are satisfied, our compiler rewrites the IR for some hardware-specific **transformations**. Finally, our compiler **lowers** the IR to a format ready for code generation.

In the rest of this section, we will discuss these three phases: analysis, transformation, and lowering, respectively.

4.1 Analysis

As mentioned above in Section 3.1 and Section 3.4, cyclic dependences among the combinational logic are prohibited. Since loops are not supported, cyclic combinational logic within a single stage is inherently prevented. Therefore, the compiler focuses on detecting cyclic dependencies in the inter-stage combinational logic.

The compiler inspects all the cross-stage references. For each instance where a combinational expression in one stage references a combinational expression from another stage, the compiler adds a dependency edge from the referencing stage to the referenced stage to construct a dependency graph. For example, the arithmetic operations in Figure 4 and Figure 5 are considered combinational, and corresponds to an edge in the graph. However, the `async_call` and `bind` expressions are considered sequential, which will **not** be added to the dependency graph.

Once the graph construction is done, the compiler performs a topological sort: iteratively, it selects and removes a vertex (stage) with no incoming edges from the graph, along with all its outgoing edges, until the graph is empty. If at a certain iteration no such vertex can be found, it indicates that cyclic combinational dependences exist among the stages, and the compiler reports an error.

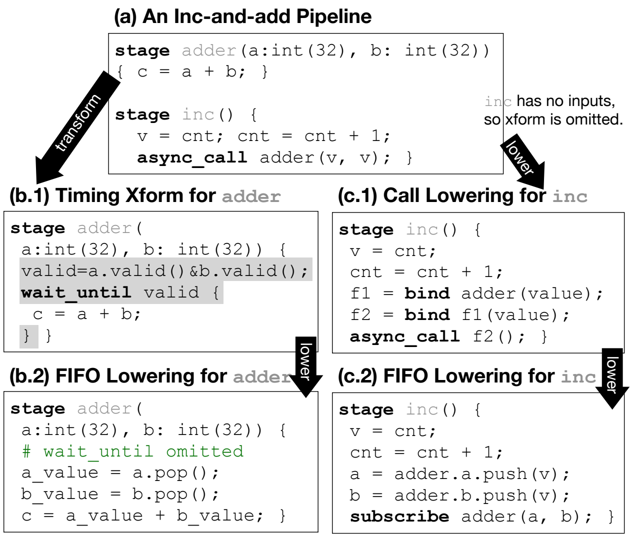


Figure 7: An example for compiler timing transformation and FIFO lowering.

Once the topological sort is done, this order is preserved for further simulator generation (see Section 5 for more details).

4.2 Transformation

We developed two specialized transformations for Assassyn that are especially useful to abstract away the low-level hardware implementation details.

Timing Control: Unlike software programming, where the data are all immediately available, hardware requires developers to manually manage the timing of data arrival. To hide this low-level detail, our compiler will by default wrap all the function bodies with a `wait_until` statement. As shown in Figure 7(b.1), the `wait_until` statement checks if all the operands in the stage buffer are valid. If any operand is invalid, this `adder` event cannot proceed. Developers can also use a `#static_timing` tag on stages to disable the transformation, as shown in Figure 5(b).

Arbiter Generation: There are two key constraints that differentiate hardware design from software programming:

1. **Resource allocation:** Each function/stage can only be called/activated once in each cycle, because dedicated on-chip resources are allocated to each pipeline stage;
2. **Register write:** A register can only be written once in each cycle, and the written value will not take effect until the very end of the current cycle.

Therefore, to evade these issues, the compiler will automatically detect the functions with multiple callers and generate an arbiter for them. As it is shown in Figure 8, both the `EX` and `MA` activate the `WB` stage to commit the results. However, these activations are not guaranteed to be mutually exclusive within a single cycle. If they both activate stage `WB` in a same cycle, they will not only activate `WB` twice, but also write to `WB`'s stage buffer twice, which leads to an undefined behavior. Therefore, an arbiter is generated among these three stages so that two upstream stages write data to separate sets of stage registers, and the state machine determines which value to commit. We currently support `#round_robin` and `#priority_arbiter` tags, allowing developers to decide strategies.

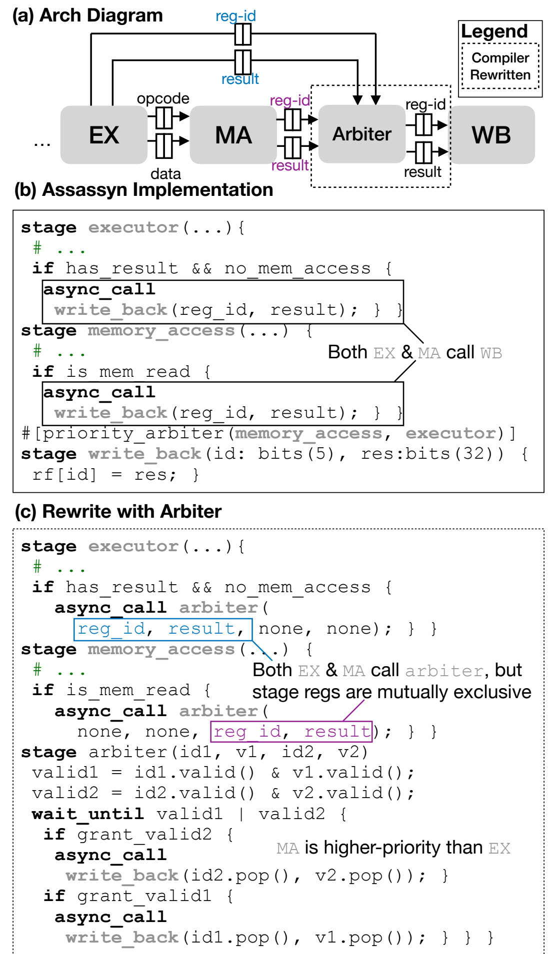


Figure 8: An example for compiler-generated arbiter.

In this case, in an in-order CPU, `MA` executes an earlier instruction, so it has a higher priority than `EX`.

4.3 Lowering

Recall that, as discussed in Section 2.2, FIFOs are adopted as our stage buffers. Therefore, we need to explicitly represent FIFO push and pop in our IR for code generation.

Function Binds to Pushes. To maintain a unified interface for compiler implementation, our compiler first rewrites all the multi-argument function calls and binds to single operand binds, and then replaces the function call itself with the bound handles. As lowering rewriting shown from Figure 7(a) to to Figure 7(c.1), the `async_call` statement is later replaced by two `bind`s, `f1` and `f2`, and then call the fully bound handle, `f2`. After this step, all the function binds will be replaced by FIFO pushes, and the function call will be replaced by event `subscription`s, as shown in Figure 7(c.2).

Function Pops. When activating a function or stage, the values in the FIFO buffers should be popped so that the next set of inputs is available at the head of the FIFOs for the next cycle. As shown in Figure 7(b.2), for the functions that implicitly use all their operands, our compiler will inject FIFO pop at the beginning of the `wait_until` body. The FIFO pop statements do not necessarily pop all the input arguments of a function. For example, as shown in

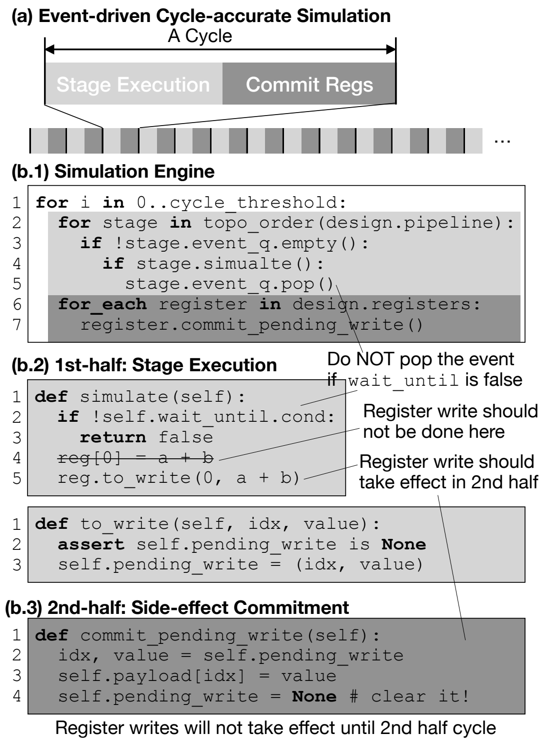


Figure 9: Assassyn-generated cycle-accurate simulator

8(c), when the generated arbiter grants execution, only the subset of the involved operands are popped.

5 Code Generation

After transforming and lowering the IR, the final step is to generate code for both the simulator and the RTL implementation. Translating the logic within each stage is straightforward, as our high-level functional programming interface naturally maps to the intended program behavior. Therefore, this section primarily focuses on the runtime support for hardware simulation, and the microarchitectural support to connect pipeline stages and generate the RTL implementation.

5.1 Simulator Generation

Figure 9(a) overviews the structure of an Assassyn-generated cycle-accurate simulator: A simulator engine drives the stage executions as well as register commitments that occur in each cycle.

Cycle-Accurate Event-Driven Simulation: As illustrated in Figure 9(b.1), in each cycle, the simulation engine traverses all the pipeline stages of the hardware design in the topological order discussed in Section 4.1. This ensures that all the cross-stage combinational references access well-defined values.

For every cycle, the simulation is divided into two phases: *stage execution* for simulating the behaviors of each stage, and *register commitment* to update the values of the registers.

Stage Execution: The first phase simulates the combinational logic within each stage. Figure 9(b.1) shows that the simulation engine traverses the `event_q` of each stage, and invokes the behavioral simulation function. The return value of each simulation function is determined by the `wait_until` condition. If true, this event will be cleared, and vice versa.

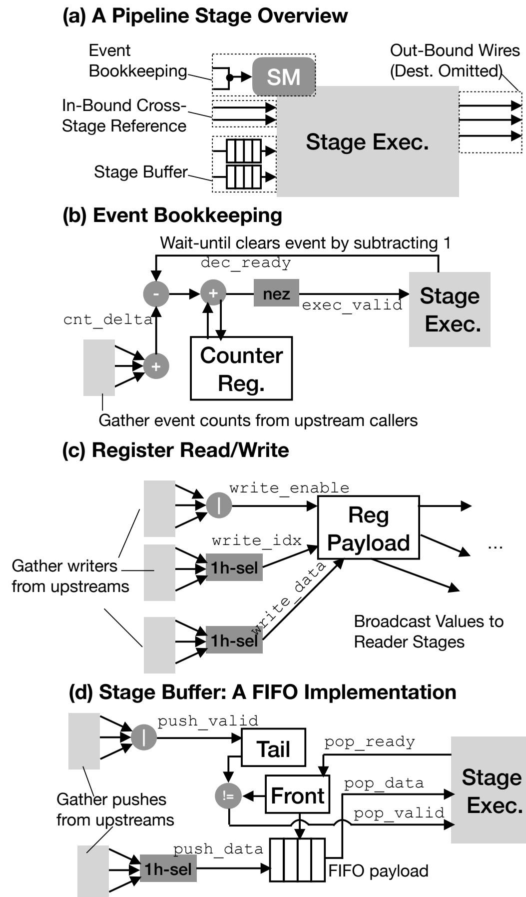


Figure 10: The μ-architectural support for RTL generation.

Register Commitment: As it is shown in Figure 9(b.2) line 4, during the stage execution phase, values written to registers cannot take effects immediately. Instead, it writes to each register's `pending_write` bookkeeping by invoking the `to_write` runtime API. This `to_write` API also enforces that each register can only be written once in each cycle. If a register is written more than once, an error will be thrown to terminate the simulation, indicating a mistake in the architectural design. All these pending writes will be committed to the registers in the second phase of a cycle, and be cleared for the subsequent cycles' simulation.

Randomization: Ideally, the order of executing stages in each cycle should not affect the simulation result. On the other hand, serialized event simulation cannot capture the full details of hardware's concurrency. Therefore, we provide a runtime flag to optionally shuffle the order of the stages without breaking the topological dependences to emulate the non-determinism.

5.2 RTL Generation

Generating RTL implementations essentially maps each aspect of the high-level abstraction to highly efficient micro-architectural components, as overviewed in Figure 10(a).

Combinational Logic: As discussed in Section 3.1, each stage's function body is composed of acyclic arithmetic operations, so it is simple to map each operation to `wire`d combinational logic in RTL.

Table 1: Manual Designs

Target Design	Reference
Priority Q [12]	Manual Impl.
In-order CPU	Sodor [3]
Out-of-order CPU	
Systolic Array	Gemmini [28]

Table 2: HLS-generated Designs from MachSuite [58]

Application	Data Size
ellpack	n=494,m=10
stencil-2d	img=128^2,f=3^2
radix-sort	n=2048,m=16
kmp	n=32000,m=4
merge-sort	n=2048

All the cross-stage combinational references can be mapped to pin ports that connect input/output values among `modules`.

Event Bookkeeping & Wait-until: We use a counter-based state machine associated to each pipeline stage to enable the conditional stage activation and event clearance. Specifically, as shown in Figure 10(b), each stage's wait-until condition is wired into this state machine to *decrease* the counter, and all the signals from upstream callers to this stage will be gathered by *addition*, rather than *or*, to ensure no event is missed and increase the counter.

Register Read/Write: The value of register writes will not take effect until the next cycle, so we use non-block assignment (<=) to write the registers. Moreover, as discussed above, a register can be read any number of times in each cycle, while only one write is allowed. Therefore, we use an or-operation to gather all the writers' write-enable signal, and conduct a one-hot selection to determine which value is written to the register. This similar technique is also applied to FIFO pushes as shown in Figure 10(d).

FIFO as Stage Registers: As discussed in Section 2.2, to ensure the generality of our language, we adopt FIFOs as our stage register. These FIFOs can be parameterized by data types determined by the data enqueued and buffer sizes determined by the `fifo_depth` API mentioned above, allowing developers to adjust the data arrival timing, consumption rate, and buffering. We implemented a penetrable FIFO as our template design, and this FIFO will fall back to a stage register when `fifo_depth(1)` is given.

See **Q4** in Section 7 for more details on the area overhead of these components discussed above.

6 Evaluation Methodology

Implementation: The current Assassyn frontend is embedded in Python by overloading the operators. By tracing the Python program execution, the hardware intermediate representation is recorded in an abstract syntax tree (AST). Then this AST is fed to our backend (implemented in Rust) for compiler transformations and code generation for both simulators and RTL implementations. The generated cycle-accurate simulators are in Rust, and the generated RTL implementations are in SystemVerilog.

Designs:[3] We select 8 representative reference designs to stress Assassyn. 3 of them are handcrafted RTL implementations, 5 of them are HLS-generated from MachSuite [58] as shown in Tables 1 and 2. We implemented a priority queue in SystemVerilog; the reference design of CPU and systolic array are from the latest Chipyard GitHub release [59]; all the HLS workloads are from Bambu [55]'s.

Software Platform: All the Rust codes, both the Assassyn compiler backend, and the Assassyn-generated simulators, are compiled by Rust 1.81.0. To simulate the Verilog, we use Verilator `v5.027` to compile the SystemVerilog, and the generated C++ simulators are compiled by GNU GCC-11.4.0.

[3]All the Assassyn-related infrastructures are are available at https://github.com/Synthesys-Lab/assassyn

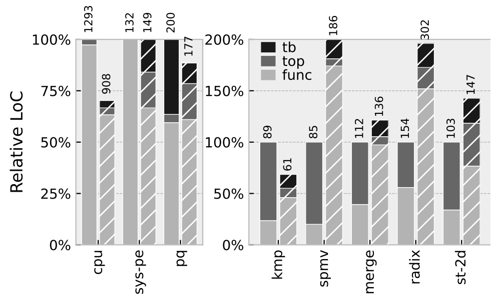


Figure 11: Lines of code breakdowns compared to reference designs, with absolute LoC above. Unhatched is the reference design, and hatched is Assassyn. (Q2)

We use Bambu [55] as our HLS baseline. All the HLS designs are generated by their `bambu-v0.9.7.AppImage` release, and simulated by Verilator. To make a fair comparison, we assume these HLS-generated designs can make fully pipelined exclusive scalar memory read/write with one-cycle latency.

To estimate the chip area of the given RTL implementation, including manual, HLS-generated, and Assassyn-generated, we use Yosys [74], accompanied with ASAP7 [22] technology library, to synthesize the RTL implementations, with all the memory-related modules excluded by a `(*blackbox*)` directive.

All the lines of code (LoC) are counted by feeding related files to `cloc` [2]. Then we manually characterize the semantics and functionality of each part of the code into 3 categories: module, top, and testbenches.

Hardware Platform: All the simulator performance reported below are single-thread, running on an AMD EPYC-7763 CPU.

Takeaway: All the chosen third-party tools and libraries are open-source to maximize our reproducibility. We plan to submit for artifact evaluation release our open-sourced infrastructure upon acceptance.

7 Evaluation

We evaluate three main aspects of Assassyn: the expressiveness of its abstraction, the quality of the generated RTL implementation, and the fidelity and performance of the generated simulator. The key results are:

- Assassyn's abstraction is expressive enough to program a wide range of hardware designs, from component modules, to application-specific accelerators and an end-to-end CPU.
- The generated simulators perfectly align with the RTL simulation results, while achieving 2.2-8.1× speedup.
- The generated RTL achieves near-handcrafted quality in terms of area, while requiring only 70% of lines of codes.

Next, we will in detail explain these key results by comparing Assassyn with both hand-crafted RTL, and HLS-generated designs on several representative workloads.

Q1. How expressive is Assassyn's abstraction?

Tables 1 and 2 show the diverse target designs we stress Assassyn to compare with both handcrafted, and HLS-generated designs. Each design showcases unique design and implementation challenges to highlight the effectiveness of Assassyn's abstraction.

For example, CPU is nearly a linear pipeline with complex inter-stage controls. Sequential communications between stages are expressed in asynchronous function invocations, and the inter-stage controls are in combinational cross-stage references.

Systolic array, exemplifying a dataflow architecture, presents a unique challenge in that each PE gathers data from multiple sources. Our *function bind* abstraction effectively enables expressing this architectural paradigm.

Notably, when manually mapping imperative C code to Assassyn for HLS comparison, we observe an interesting pattern: each Assassyn function resembles a basic block in a control flow graph, while `async_call` acts as a branching mechanism between these blocks. This correspondence not only highlights how our abstraction bridges the imperative programming model with hardware design and implementation, but also unveils the potential of leveraging Assassyn as a novel HLS backend.

Q2. How well does Assassyn mitigate the difficulties of hardware design and implementation?

Figure 11 presents a comparison of lines of code (LoC) for each workload between designs implemented with Assassyn and their corresponding reference implementations, which are either handcrafted RTL or HLS-generated code.

Handcrafted RTL: Assassyn requires only 70% of the LoC of the reference RTL when the design is as complicated as a single-issue CPU; for simple components, the LoC is comparable to Chisel RTL. We excluded all the highly overengineered common modules in Chipyard-related reference designs for Sodor CPU, and Gemmini systolic array, or the LoC comparison will be badly skewed. For example, Chipyard overengineered a unified testbench for all the CPU-based designs in the `generator` directory, and Sodor adopts a comprehensive implementation of state control registers (CSR) from `roketchip`. These LoC savings are primarily attributed to the language abstraction provided by Assassyn. Traditional RTL implementations involve redundant code for pin declarations and connections across hierarchical synthesis, whereas Assassyn simplifies these aspects through function calls and cross-module references.

HLS-generated Design: Our Assassyn-programmed workloads require, on average, only 1.26× the LoC of the MachSuite C code, with testbench `harness` included, to implement these application-specific accelerators. Two outliers, `spmv` and `merge` require more than 2× LoC in total. `spmv`'s kernel alone even demands 11× LoC. `spmv`'s kernel complication stems from three memory operations, 2 loads and 1 write, in its loop body. The exclusive memory read-/write constraints necessitates careful state machine management to schedule the memory accesses. `merge` suffers from a similar situation. Nevertheless, Assassyn's full control over the underlying hardware's micro-architecture and pipeline stages enable better performance and area tuning. As a result, as shown in Figure 12, we achieve an order of magnitude improvement in area-normalized performance over HLS.

Q3. What is the quality of Assassyn-implemented hardware?

As shown in Figure 12, Assassyn-programmed designs achieve comparable performance per area to handcrafted designs, while delivering up to 32× and by mean 6× over HLS-generated designs. Below, we analyze these results by examining both performance and area characteristics.

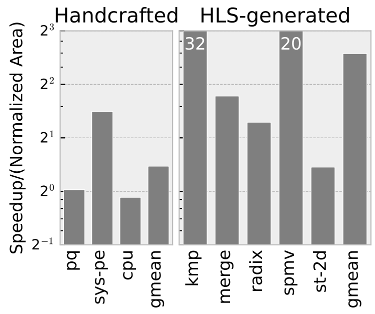


Figure 12: Area normalized performance (Q3)

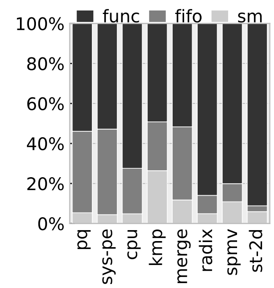


Figure 13: Area breakdown (Q4)

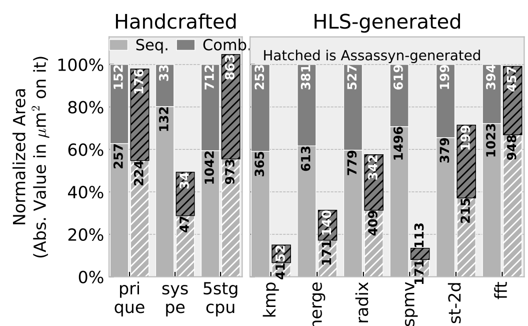


Figure 14: Area compared with reference designs (Q3)

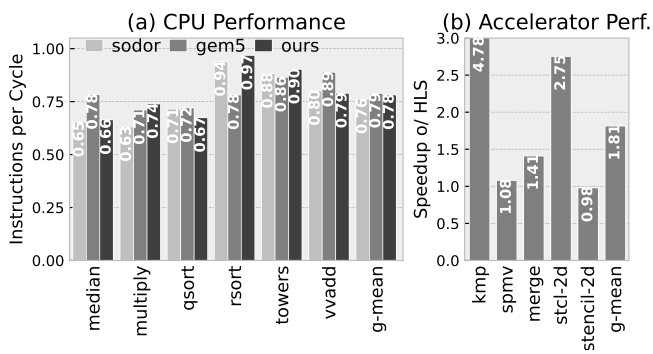


Figure 15: CPU/HLS performance comparison (Q3)

Performance: The performance of the priority queue and the systolic array are estimated by their pipeline initial interval (II). Because handcrafted references and the Assassyn-programmed ones achieve the identical desired II, we assume they have the same performances. Therefore, we only simulated the Sodor CPU to evaluate the performance, by running six workloads from the Sodor project folder. Our implementation achieves slightly better performance, 2.6% higher IPC, than Sodor CPU as shown in Figure 15(a), because we implemented an always-take branch prediction, which introduces around 3% area overhead as shown in Figure 14.

As shown in Figure 15(b), when comparing with equal provisioned HLS code, Assassyn-programmed designs achieve, on average, 1.8× speedup over HLS-generated designs. The speedup primarily stems from two factors: 1) our full control over the underlying pipeline stages and micro-architecture, allowing for more aggressive pipeline scheduling compared to HLS, and 2) smarter, human-driven optimizations. In `kmp`, the length of the pattern string is only 4, so we implemented a brute force string match to avoid excessive memory access, and complicated control. In `radix_sort`, instead of allocating the radix brackets in SRAM, we use 16 registers as our radix brackets. This design decision trades off chip area and the number of iterations required to scan the entire array, while also eliminating two memory accesses for bracket accumulation. This simplification reduces the complexity of the state machine that manages exclusive memory reads and writes in the innermost loop body. In `merge_sort`, our implementation adopts an infinite sentinel to maintain a unified interface of popping merged elements when one side is exhausted, which simplifies the state transition.

Area Cost: The area comparison is shown in Figure 14. Our Assassyn-implemented designs achieve comparable area to handcrafted designs with similar functionality (CPU and priority queue). Systolic PE is an outlier, because Gemmini's [28] systolic array is highly flexible for both output and weight stationary models, which introduces extra combinational area to control the state machine inside the PE. On the other hand, HLS inevitably suffer from area overhead caused by HLS tools, and our Assassyn-programmed designs achieve an average area savings of 70%.

Q4. What is the language abstraction overhead of Assassyn?

To better understand our language abstraction overhead, we characterize the area of two main Assassyn-generated architectural components, the FIFOs serving as stage registers, and the counter stage machine serving as stage execution bookkeeping. The area breakdown shown in Figure 10 are counted by synthesizing each standalone component, and sum them up, because the synthesis tool flattens all the architectural hierarchies for more aggressive synthesis optimizations, which loses the hierarchical information for components. This approach may slightly enlarge the area of each component. Their area breakdowns are shown in Figure 13. For `spmv`, and `stencil-2d`, the functionality area is mainly occupied by the multiplication and accumulation unit, while for `radix`, the functionality area is mainly spent on the bracket registers.

The stage registers are inevitable when designing and implementing pipelined architectures. Their areas can be easily tuned by calling the `fifo_depth` API. When area 1-depth is given, the FIFO will fall back to a single stage register. These stage buffers occupy around 20%-40% of the area in control-heavy designs, e.g. CPU, priority queue, and merge sort.

In most of the workloads, another language-generated component, the counter state machine is a modest overhead (consumes less than 5% of the total area). An outlier, `kmp`, is too simple to dwarf this component — as shown in Figure 14, the absolute area is less than $100\mu m^2$. Though redundant, in many static-timing designs, e.g. systolic array, such state machines are still generated to maintain a unified interface for both simulation and RTL generation, which can be eliminated in our future version.

Q5. What is the quality of the generated simulator?

We evaluate three key aspects of our Assassyn-generated simulators, the alignment, the performance, and debugging.

Alignment: As discussed in Section 2.2, the transposed correspondence between the event simulation traces and the waveform activation enables a perfect alignment between the simulation-based modeling and the RTL implementation. Across all our target designs, all the cycles counts from Verilator simulated RTL exactly match our Assassyn-generated Rust simulator. In contrast, aligning

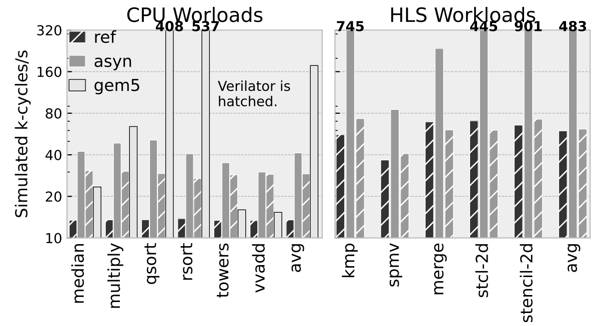


Figure 16: Assassyn-generated cycle-accurate simulator compared to Verilator-generated Verilog simulation, and simulation-based modeling (Q5)

gem5-simulated results with an actual RTL implementation proves challenging even in a design as simple as a single-issue CPU.

To demonstrate, we configured a minimized in-order, single-issue, and one-cycle memory access CPU in gem5 23.0. As shown in Figure 15, while the three implementations — sodor, gem5-simulated, and ours — achieve similar mean performance, gem5's results show significant fluctuations across different benchmarks. This suggests that the similar mean performance is merely coincidental, resulting from offsetting variations rather than consistent behavioral alignment with RTL. Our detailed analysis of execution traces revealed specific sources of misalignment. In `median` and `vvadd`, gem5 CPU outperforms ours because its fetch stage can access branch execution results within the same cycle — an design that would lengthen the combinational critical path in actual hardware. Conversely, gem5 underperforms on `rsort` due to a missed bypassing opportunity: when instruction A is decoded and depends on instruction B in writeback, B's result remains invisible to A until next cycle while bypass registers already have been flushed and occupied by other newer instructions in EX and MA. Such subtle discrepancies can hardly be discovered through extensive coordination between design and implementation teams, while it is naturally aligned in our framework.

Performance: As shown in Figure 16, our Assassyn-generated cycle-accurate simulator implemented in Rust is 2.2× faster than the Verilator-generated simulator on CPU simulation, and has 8.1× speedup over HLS ASIC simulation. This speedup comes from the domain knowledge of simulating pipeline stages, which significantly simplifies the architectural simulation model. A generic SystemVerilog simulation/modeling typically involves a rather complicated process to 1. maintain the event queue of each timescale; 2. determine the active and inactive code regions in a fine-grained style; 3. compute the logics; 4. cleanup each cycle and move time forward [4]. Our two-phase model discussed in Section 5.1 can rapidly determine the active and inactive code region in the granularity of each pipeline stage to save simulation time.

For workloads fewer than 10k cycles like `vvadd`, `tower`, and `median`, gem5's initialization overhead hinders its performance compared to both Assassyn and even Verilator-generated simulator. However, for longer-running workloads like `qsort` and `rsort`, gem5 achieves an order of magnitude speedup once this overhead is amortized. Gem5 excels in raw simulation speed, but our Assassyn-generated simulators offer a unique cycle-exact correspondence

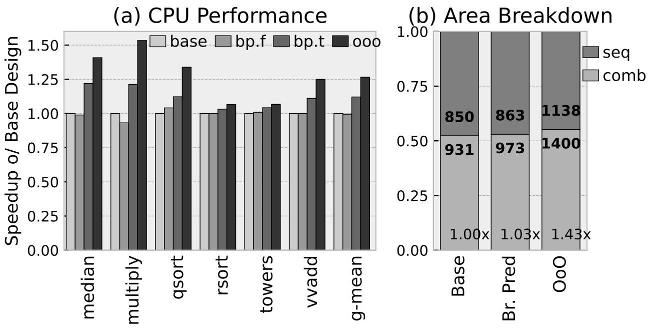


Figure 17: CPU performance by incrementally enabling branch prediction, and out-of-order. `bp.f` is always not taken, and `bp.t` is always taken.

with RTL implementation, which will enable precise debugging and facilitate seamless transition from design to implementation.

Debugging: Conventional Verilog simulation typically involves massive concurrency and non-determinism, making it hard to locate the mistake, while the serialized event-driven simulation, with operations within the same stage tightly coupled, significantly simplifies tracing execution and analyzing expected behaviors. Most behavioral bugs can be easily found at this phase.

Q6. How could Assassyn facilitate a seamless architecture design and implementation?

A key benefit of Assassyn is enabling seamless transition from architectural design to RTL implementation. Design decisions can be rapidly evaluated for both performance impact and hardware cost. We demonstrate this advantage through an progressive CPU design case study.

We incrementally developed several CPU variants. Starting from a fully interlocked 5-stage single-issue in-order base design, we extended it with branch prediction and ultimately implemented an out-of-order (OoO) version with branch prediction. For the branch prediction study, we implemented two simple strategies: always-taken (bp.t) and always-not-taken (bp.f). The performance impact of each mechanism is shown in Figure 17(a), and the generated RTL can be immediately synthesized to inspect the cost, as shown in Figure 17(b). The always-not-taken predictor shows limited performance improvement because most branches in these workloads are taken, particularly loop branches that jump back to the loop header. This behavior is quantified by the success rate of the always-taken predictor shown below:

median	mul	qsort	rsort	towers	vvadd
59.4%	90.6%	64.9%	76.2%	85.7%	71.8%

Both branch predictors require very near on-chip area, so we only report the always-taken predictor area, which improves the performance by 1.12× and introduces around 3% area overhead.

OoO Execution: Moreover, our framework scales to designs as complicated as an out-of-order CPU with always-taken branch prediction. It achieves 1.26× speedup over the base design, and introduces 1.43× area overhead. To understand this performance gain, we profiled each workload execution. Instructions are dispatched to reservation station in almost every cycle. An outlier is `qsort`, which introduces 2.1% dispatch idle, because of the limited size of the reservation buffer size. Instructions can retire after 3 cycles when they are on the correct code path, and issuance unit only is only idle for 5.4% of the cycles, which is mostly caused by branch misprediction. In more than 99% of misprediction, there is at most one instruction mistakenly dispatched by the always-taken branch prediction, because we prioritize the branch instruction execution on the reservation stations. To sum up, all the profiling above suggests OoO effectively exploits the CPU pipeline utilization.

When developing, Assassyn illustrates a key advantage: Analogous to software application development, which follows a "algorithm+data structure" paradigm, our Assassyn-implemented out-of-order CPU follows a "pipeline logic+bookkeeping" approach. This abstraction naturally separates the core pipeline functionality from the state management required for out-of-order execution, making the code base more maintainable.

8 Discussion

The fundamental challenge in architectural design and implementation stems from the complexity of RTL programming, which led to the separation of simulation and implementation codebases, while Assassyn addresses this challenge by reproposing a programming paradigm to unify the simulation and implementation.

8.1 Related Works

Prior hardware modeling works [14, 15, 17, 43, 80] still remain highly disconnected between the simulation and implementation. The prior work closest to our goal should be PyMTL [46] and Gem5+RTL [47]. PyMTL aims at offering a unified simulation-based modeling framework to integrate components with different level of implementation, from functional to RTL, but this still relies on developers to manually implement of a same component multiple times. gem5+RTL allows developers to integrate their extended components written in RTL to a full-system simulation. In contrast to the framework discussed above, the primary goal of Assassyn is even more aggressive, unifying the cycle-accurate simulation and the RTL implementation.

Meanwhile, high-level RTL generators target only a limited subset of architectures, including but not limited to general-purpose CPUs [17, 77, 78] or domain-specific accelerators [27, 39, 68, 72], or address individual challenges in hardware description — such as placement [67] *or* timing [50]. In contrast, Assassyn seeks an *all-in-one* approach for design and implementation by carefully rethinking abstraction through the lens of software language evolution.

Beyond the scope of this programming paradigm, our work reveals two boarder insights on hardware description language and architectural design compared to prior related works.

Analogous to software programming, we characterize conventional SystemVerilog as assembly code, and Chisel [6] serves as a intrinsic wrapper (or syntactical sugar) that encapsulates many common uses of RTL programming, targeting an open-source IR infrastructure [32], CIRCT (a.k.a. FIRRTL), to mitigate the programming difficulties. These prior works still adhere to the circuit graph abstraction, and pin connections. Meanwhile, software languages evolved beyond assembly by carefully trading-off the unnecessary expressiveness. A famous example is the deprecation of the `goto-statement` in modern languages: by disabling the excessive flexibility of branching across the basic blocks, programmers' productivity and code quality were significantly improved. The compiler can also make stronger assumptions to apply more aggressive optimizations. **Assassyn represents a first step toward a "C-like" abstraction for hardware design and implementation.** Similarly, by carefully constraining the programming model to event-driven patterns, and binding the dataflow across the pipeline stages, a higher level of abstraction that retains the expressiveness to implement many practical architectures is achieved.

Moreover, though many prior works [20, 42, 44, 56, 72, 73] already demonstrated that domain-specific accelerators can be composed by connecting spatial processing elements, our work suggests an even more fundamental principle: **Spatial processing element is all you need** for pipelined architectural construction. Each pipeline stage can be viewed as a spatial processing element, and its functionality can be programmed within an Assassyn function. A pipelined architecture can be viewed as a spatial arrangement of these processing elements connected by dataflows. This principle becomes particularly striking when considering seemingly sequential architectures like CPUs — unlike spatial dataflow accelerators that typically employ an array of homogeneous processing elements, CPU pipelines are constructed by connecting multiple heterogeneous stages, yet still fundamentally adhere to this spatial arrangement paradigm. This principle may lead to a more agile design, implement, and evaluation flow for new architectures.

8.2 Future Works

Frontend: When implementing the `radix_sort` and `merge_sort`, we found it particularly challenging to manually manage the state of execution and transition across the different phases of the algorithm. It will be highly desirable to have better abstraction to program different code regions that share the same inputs but execute under different conditions, and the transitions across these conditions can be easily and clearly describe like imperative programming.

Backend: As a programming language, Assassyn occupies a unique position, which is both *domain-specific* in its focus on hardware design and implementation, and *general-purpose* in its expressiveness of the architectural construction. *"Domain-specific"* typically implies that additional domain knowledge enables more aggressive automated optimizations [8, 18, 38, 57, 71, 82] on the programmed *"general-purpose"* architecture designs. As discussed above, our language naturally encodes: 1. the clear boundary of each pipeline stage, and 2. the clear separation between the combinational and sequential logic. This domain-specific knowledge opens up promising optimization opportunities to automatically 1. find the critical path of a design before synthesis; 2. verify the intra-stage and inter-stage stage machine footprint for complicated designs.

Integration: Assassyn-generated RTL maintains clear correspondence to high-level design intentions, making it more readable than conventional HLS-generated RTL for both human and machines. This quality positions Assassyn as a valuable tool for generating high-quality training datasets for AI for hardware design.

9 Conclusion

We introduced Assassyn, a *unified*, *general-purpose*, and *high-level* programming framework for hardware design and implementation, offering a fresh perspective on describing hardware pipelines. Our evaluation highlights the framework's advantages in terms of expressiveness, productivity, and the quality of hardware generation, demonstrating its potential as a transformative tool in the hardware design space. More broadly, this work establishes a foundation for a new paradigm in hardware description languages, bridging the disconnection between the high-level design and the low-level implementation. In doing so, it opens the door to future research in automated design optimizations and reimagines the way we approach hardware design and development.

Acknowledgments

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